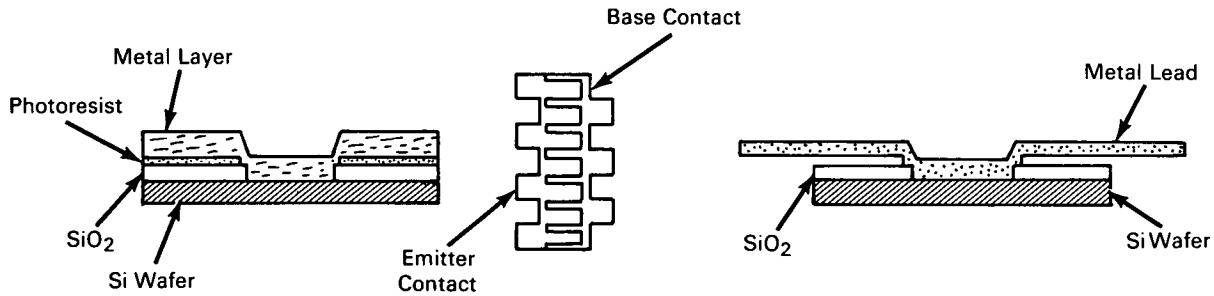
NASA TECH BRIEF

Integrated Metal Transistor Leads



The problem:

In the conventional manufacture of transistors, large pellet bonding terminals are required as targets for the bonded lead wires and contribute to device capacitance. Additionally, the incidence of bonding lead wires having different lengths is a factor that results in an increased inductance to those emitters being fed by the longer wires and subsequent degeneration in their injection.

The solution:

A technique that makes the metal leads integral to the transistor wafer. This appreciably reduces capacitance in the device, thereby increasing its efficiency.

How it's done:

After defining the base contacts in the oxide and depositing Au in the openings, the wafer is again coated with a photoresist and an opening is made in the resist. A layer (60,000–100,000 Å) of Al is then evaporated over the surface of the wafer, forming the composite structure shown in the left figure. The metal is next coated with photoresist and defined by electrolytic etching to produce a pattern on each pellet in the form shown in the center figure.

The wafer is next scribed on each side by standard scribing techniques to assist separation of the individual pellets, accomplished by placing the wafer in hot benzene sulphuric acid which dissolves all the photoresist, leaving pellets like that shown in the right figure.

Notes:

1. Measurements made on TA2675 devices fabricated with integral leads and fabricated with wire-bonded leads showed a 26% capacitance reduction in the integral lead device.
2. In using integral leads, length of the bond wires is controlled by photolithographic techniques, assuring equal inductance to the pellet.
3. No additional documentation is available. Inquiries may be directed to:

   Technology Utilization Officer
   Goddard Space Flight Center
   Greenbelt, Maryland 20771
   Reference: B68-10518

Patent status:

No patent action is contemplated by NASA.

Source: E. T. Casterline and D. R. Carley
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Category 01